***Abstract* –**

Reducing power consumption is an indispensable quest in our modern world.  With the ever-present need for portable devices like smartphones and laptops, minimizing energy usage dissipation has become a central challenge. This pressing concern has driven the development of innovative techniques to curb power loss in Very-Large-Scale Integration (VLSI) chips, the workhorses of modern electronics.

The insatiable demand for portable electronics has propelled low-power design to the forefront of VLSI development. While CMOS technology offers scaling advantages and inherently low static power dissipation, challenges persist. Despite significant increases in transistor count and operating frequency, modern processors grapple with leakage currents similar to their decade-old counterparts. Understanding the various power dissipation mechanisms

However, the pursuit of ever-smaller, faster, and lower-power chips necessitates a delicate balancing act between power consumption, performance, and chip area. This paper explores the multifaceted problem of power dissipation in CMOS circuits, delving into both dynamic and static power sources .

This review underscores the critical role of low-power design in shaping the future of VLSI technology. Through continuous exploration of innovative design techniques, we can create energy-efficient chips that meet the ever-growing demands of modern computing while ensuring a sustainable future

Tittle - re

view on low power design on VLSI CHIPS with current trends

Abstract – ChatGPT

Into – what is it about methods

* Power dissipation CMOS (dynamic)

Switch --

Short skt --

Lekage power

\*glitching --

Compare(I7 2013 vs I7 2023)

Concusion

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The surging popularity of portable and wireless personal computing devices has thrust power consumption into the spotlight as a critical design concern. Alongside area and performance optimization, minimizing power dissipation has become a central challenge in VLSI design. While advancements continue in processor capabilities, as exemplified by the latest Core i7 processors, efficient power management remains paramount.

Understanding the different types of power dissipation in traditional CMOS logic circuits forms the foundation for effective reduction strategies. Several high-level digital circuit designs prioritizing low-power and low-voltage operation have emerged, serving as valuable examples for achieving this goal [4].

Interestingly, the battle against power dissipation intensifies when comparing processor generations. The 14th generation Intel Core i7 processors (I7-14xxx) offer significant performance improvements compared to the 4th generation (I7-4xxx). This is partly achieved through a more advanced 10nm fabrication process, which inherently leads to higher leakage currents. However, the 14th generation processors likely employ counteracting measures like lower operating voltages and potentially incorporate leakage reduction features. These advancements aim to achieve similar or even lower overall power consumption despite the performance gains, showcasing the ongoing efforts to tackle power dissipation in ever-evolving VLSI technology.

//introduction

In order to develop techniques for minimizing power dissipation, it is essential to identify various sources of power dissipation and different parameters involved in each of them. Power dissipation may be specified in two ways. One is maximum power dissipation, which is represented by “peak instantaneous power dissipation.” Peak instantaneous power dissipation occurs when a circuit draws maximum power, which leads to a supply voltage spike due to resistances on the power line. Glitches may be generated due to this heavy flow of current and the circuit may malfunction, if proper care is not taken to suppress power-line glitches. The second one is the “average power dissipation,” which is important in the context of battery-operated portable devices. The average power dissipation will decide the battery lifetime. Here, we will be concerned mainly with the average power dissipation, although the techniques used for reducing the average power dissipation will also lead to the reduction of peak power dissipation and improve reliability by reducing the possibility of power-related failures. In CMOS circuits, power dissipation can be divided into two broad categories: dynamic and static. Dynamic power dissipation in CMOS circuits occur when the circuits are in working condition or active mode, that is, there are changes in input and output conditions with time. In this section, we introduce the following three basic mechanisms involved in dynamic power dissipation:

• Short-circuit power: Short-circuit power dissipation occurs when both the nMOS and pMOS networks are ON. This can arise due to slow rise and fall times of the inputs as discussed in

• Switching power dissipation: As the input and output values keep on changing, capacitive loads at different circuit points are charged and discharged, leading to power dissipation. This is known as switching power dissipation. Until recently, this was the most dominant source of power dissipation. The switching power dissipation is discussed in

• Glitching power dissipation: Due to a finite delay of the logic gates, there are spurious transitions at different nodes in the circuit. Apart from the abnormal behavior of the circuits, these transitions also result in power dissipation known as glitching power dissipation.

//short – circuit

Short-Circuit Power Dissipation When there are finite rise and fall times at the input of CMOS logic gates, both pMOS and nMOS transistors are simultaneously ON for a certain duration, shorting the power supply line to ground. This leads to current flow from supply to ground. Short-circuit power dissipation takes place for input voltage in the range Vtn < Vin < Vdd − | Vtp |, when both pMOS and nMOS transistors turn ON creating a conducting path between Vdd and ground (GND). It is analyzed in the case of a CMOS inverter as shown in Fig. 6.2. To estimate the average short-circuit current, we have used simple model shown in Fig. 6.3. It is assumed that τ is both rise and fall times of the input (τ r = τf = τ ) and the inverter is symmetric, i.e., βn = βp = β and Vtn = −Vtp = Vt . As the clock frequency decides how many times the output changes per second, the short-circuit power is proportional to the frequency. The short- circuit current is also proportional to the rise and fall times. Short-circuit currents for different input slopes are shown in Fig. 6.4. The power supply scaling affects the short-circuit power considerably because of cubic dependence on the supply voltage. such a situation, the short-circuit current will be very small. It is maximum when there is no load capacitance. The variation of short-circuit current for different out-put capacitances is shown in Fig. 6.5. From this analysis, it is evident that the short-circuit power dissipation can be minimized by making the output rise/fall times smaller. The short-circuit power dissipation is also reduced by increasing the load capacitance. However, this makes the circuit slower. One good compromise is to have equal input and output slopes. Because of the cubic dependence of the short-circuit power on supply voltage, the supply voltage may be scaled to reduce short- circuit power dissipation. We may conclude this subsection by stating that the short-circuit power dissipation depends on the input rise/fall time, the clock frequency, the load capacitance, gate sizes, and above all the supply voltage.

//Switching Power Dissipation

There exists capacitive load at the output of each gate. The exact value of capacitance depends on the fan-out of the gate, output capacitance, and wiring capacitances and all these parameters depend on the technology generation in use. As the output changes from a low to high level and high to low level, the load capacitor charges and discharges causing power dissipation. This component of power dis-sipation is known as switching power dissipation. Switching power dissipation can be estimated based on the model shown in Fig. 6.8. Figure 6.8a shows a typical CMOS gate driving a total output load capacitance CL. For some input combinations, the pMOS network is ON and nMOS network is OFF as modeled in Fig. 6.8b. In this state, the capacitor is charged to Vdd by drawing power from the supply. For some other input combinations, the nMOS network is ON and pMOS network is OFF, which is modeled in Fig. 6.8c. In this state, the capacitor discharges through the nMOS network. For simplicity, let us assume that the CMOS gate is an inverter. This implies that half of the energy is stored in the capacitor, and the remaining half (1 / 2)C LVdd 2 is dissipated in the pMOS transistor network. During the Vdd to 0 transition at the output, no energy is drawn from the power supply and the charge stored in the capacitor is discharged in the nMOS transistor network. If a square wave of repetition frequency f (I/T) is applied at the input, average power dissipated per unit time is given by The switching power is proportional to the switching frequency and independent of device parameters. As the switching power is proportional to the square of the sup-ply voltage, there is a strong dependence of switching power on the supply voltage. Switching power reduces by 56 %, if the supply voltage is reduced from 5 to 3.3 V, and if the supply voltage is lowered to 1 V, the switching power is reduced by 96 % compared to that of 5 V. This is the reason why voltage scaling is considered to be the most dominant approach to reduce switching power.

//Glitching Power Dissipation

In the power calculations so far, we have assumed that the gates have zero delay. In practice, the gates will have finite delay and this delay will lead to spurious undesirable transitions at the output. These spurious signals are known as glitches. In the case of a static CMOS circuit, the output node or internal nodes can make undesirable transitions before attaining a stable value. Consider the circuit shown in Fig. 6.15. If the inputs ABC change value from 101 to 000, ideally for zero gate delay the output should remain at the 0 logic level. However, considering unit gate delay of the first gate stage, output O1 is delayed compared to the C input. As a consequence, the output switches to 1 logic level for one gate delay duration. This transition increases the dynamic power dissipation and this component of dynamic power is known as glitching power. Glitching power may constitute a significant portion of dynamic power, if circuits are not properly designed. Usually, cascaded circuits as shown in Fig. 6.16a exhibit high glitching power. The glitching power can be minimized by realizing a circuit by balancing delays, as shown in Fig. 6.16b. On highly loaded nodes, buffers can be inserted to balance delays and cascaded implementation can be avoided, if possible, to minimize glitching power

//Leakage Power Dissipation

When the circuit is not in an active mode of operation, there is static power dissipation due to various leakage mechanisms. In deep-submicron devices, these leak-age currents are becoming a significant contributor to power dissipation of CMOS circuits. Figure 6.17 illustrates the seven leakage mechanisms. Here, I1 is the re-verse-bias p–n junction diode leakage current; I 2 is the reverse-biased p–n junction current due to tunneling of electrons from the valence bond of the p region to the conduction bond of the n region; I3 is the subthreshold leakage current between the source and the drain when the gate voltage is less than the threshold voltage Vt; I4 is the oxide-tunneling current due to a reduction in the oxide thickness; I5 is gate current due to hot-carrier injection of elections; I6 is the GIDL current due to a high field effect in the drain junction; and I7 is the channel punch-through current due to the close proximity of the drain and the source in short-channel devices. These leakage components are discusse

// power dissipation topic:

The most common VLSI technology is CMOS primarily because its scaling properties and low power dissipation permit greater levels of integration than alternative technologies [10]. Since complementary CMOS logic gates require power only during signal transitions, static power dissipation is nearly eliminated. Detailed 200 Chau and Powell discussions of the power dissipation of basic CMOS logic gates can be found in [12]-[15]. Calculating the power dissipation of large CMOS circuits or entire VLSI chips is a difficult task and most current approaches involve logic or switch level simulations of the entire chip [16]-[18].

//CMOS Power Dissipation

The simplest CMOS logic dement is the inverter. As shown in figure 1, there are two main currents which flow each time the inverter's output transitions. These currents are called the dynamic, idy(t), and short circuit, isc(t), components. The dynamic component is from charging and discharging the load capacitance CL and the short circuit component is from n- and pchannd transistors conducting simultaneously as the input is transitioning. In general, any complementary logic dement will exhibit the same behavior. Note we are assuming that the power dissipation due to static leakage current (proportional to transistor size) and circuit resistances (IER) is small in comparison to the dynamic and short circuit power dissipation. For periodic signals, the average power dissipation for a single logic element as in figure 1 is defined as: Pavg = -~ lff gddidd (t) dt fo = Vdaf ida (t) tit = Vddfq (1) where T = period f = 1/T = frequency q = the charge transferred per cycle For each logic transition, the charge transferred to the load capacitor by the dynamic current is q = CL Vda. For nonperiodic switching, the average power dissipation of a single CMOS logic dement can be found by defining an activity factor: Af = average number of switchings per cycle (0 \_< Af< 1) and thus the power dissipated by a single logic element is given by: Pavg = Af[CLV2df + Vdaf forisc(t) dt 1 (2) where isc(t) = the short circuit component CL Vdaf = the dynamic current component, iay(t) A thorough discussion and analysis of short circuit power dissipation in CMOS inverters can be found in [14]. Yacoub [13] presents a method for separating the dynamic and short circuit components of general multigate CMOS circuits and finds that the short circuit component can range from 20%-50% of the total power dissipation.

## // Power Dissipation in VLSI Circuits: A Balancing Act

Power dissipation remains a critical challenge in achieving high integration levels in VLSI design. While CMOS technology offers excellent scaling properties and low power consumption, understanding the various power dissipation mechanisms is crucial for efficient circuit design.

This research explores the three main contributors to power dissipation in CMOS circuits: dynamic, short-circuit, and static power.

* **Dynamic Power:** This component arises from charging and discharging the load capacitance (CL) during signal transitions. It is primarily influenced by CL, supply voltage (VDD), activity factor (α, representing the average switching frequency), and clock frequency (f). The formula Pdyn = CL \* Vdd^2 \* α \* f captures this relationship (refer to [5, 6] for detailed discussions).
* **Short-Circuit Power:** This occurs when both PMOS and NMOS transistors conduct simultaneously during input transitions (Figure 1). This short-circuit current (isc(t)) contributes to power dissipation alongside the dynamic current (idy(t)). While generally smaller than dynamic power, short-circuit power can range from 20% to 50% of the total dissipation (refer to [13, 14] for a deeper analysis).
* **Static Power (Leakage Power):** Unlike the previous two components, static power is continuously dissipated even when the circuit is inactive. Leakage currents, influenced by VDD, threshold voltage (Vt), and transistor size, are the primary culprits. As process technology scales, leakage becomes a more significant concern, potentially consuming over 30% of total power (refer to [2]). Techniques like MTCMOS (refer to [4]) have been proposed to mitigate leakage in sleep modes.

In conclusion, achieving low-power VLSI design requires careful consideration of all three power dissipation components. By optimizing factors like VDD, transistor sizing, and circuit techniques for dynamic and short-circuit power reduction, alongside leakage management strategies, researchers can create energy-efficient circuits that pave the way for longer battery life and improved performance in portable devices.

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**Switching Power Dissipation: A Dominant Factor in Low-Power VLSI Design**

Switching power dissipation is a critical factor limiting battery life and necessitating low-power design approaches in VLSI circuits. It arises from the charging and discharging of the capacitive load at the output of each logic gate during transitions between logic states [2]. The exact value of this load capacitance depends on several parameters, including the fan-out of the gate, its output capacitance, and the wiring capacitances involved [1]. These parameters are all influenced by the underlying fabrication technology generation.

A simplified model can be used to estimate the switching power dissipation. Consider a standard CMOS inverter driving a load capacitance (CL) (Figure 6.8a). As the input to the inverter changes, the PMOS or NMOS network conducts accordingly, charging or discharging the capacitor (Figures 6.8b and 6.8c). During charging (from low to high), power is drawn from the supply to accumulate energy in the capacitor. Conversely, power is dissipated during discharging (from high to low).

While a basic formula (Equation 1 or 2) can be derived based on load capacitance, supply voltage (Vdd), and operating frequency (f), it assumes only one transition per clock cycle. In reality, logic gates can experience multiple transitions, necessitating a more nuanced approach.

The concept of the node transition factor (α) is introduced to account for the actual number of transitions occurring at each clock cycle. This refined formula (Equation 3) provides a more accurate estimate of switching power dissipation.

Furthermore, for complex logic gates, internal nodes besides the output can also undergo transitions during operation. To account for this, a more comprehensive formula (Equation 4) considers the capacitance (Ci), voltage (Vi), and transition factor (αTi) of each individual node. The summation across all nodes provides a more holistic picture of switching power dissipation in VLSI circuits.

By understanding and optimizing switching power dissipation through techniques like voltage scaling, designers can achieve significant power reduction in VLSI chips, leading to longer battery life and improved performance in portable electronic devices.

## // Glitching Power: The Pitfall of Non-Ideal Delays in VLSI Circuits

Our previous discussions on power consumption assumed gates with zero delay. In reality, gates have finite delays, and these delays can introduce unintended behavior. These unwanted transitions at the output are known as glitches.

In static CMOS circuits, glitches can occur on the output node or even internal nodes before they reach a stable logic level. Figure 6.15 serves as an example. Ideally, with zero gate delay, the output should remain at 0 when inputs ABC change from 101 to 000. However, with a unit gate delay in the first stage, the output O1 lags behind the C input. This lag causes a temporary switch to the 1 logic level for the duration of the gate delay. This unnecessary transition increases the dynamic power consumption, and this additional power is known as glitching power.

Glitching power can become a significant contributor to the overall dynamic power dissipation if circuits are not designed carefully. Circuits with cascaded stages, like the one shown in Figure 6.16a, are particularly prone to high glitching power.

Fortunately, there are techniques to minimize glitching power. One approach involves balancing delays throughout the circuit (Figure 6.16b). This ensures that all signals arrive at their destinations at similar times, minimizing the window for glitches to occur.

For highly loaded nodes (nodes driving a large number of other circuits), buffers can be inserted to balance delays. Additionally, whenever possible, designers may opt for non-cascaded implementations to further reduce glitching power.

By understanding and mitigating glitching power, VLSI designers can create more efficient circuits with lower power consumption. This is crucial for extending battery life and improving the overall performance of portable electronic devices.

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## Short-Circuit Power Dissipation: A Hurdle in Low-Power VLSI Design

Beyond switching and glitching power, short-circuit power dissipation emerges as another challenge in achieving low-power VLSI design. This phenomenon arises due to the finite rise and fall times of input signals in CMOS logic gates. During these transitions, a brief period exists where both the PMOS and NMOS transistors are partially ON simultaneously. This creates a direct path between the power supply (VDD) and ground (GND), leading to a surge in current flow.

Figure 6.2 depicts a CMOS inverter, where short-circuit current occurs when the input voltage lies between the threshold voltages of the PMOS and NMOS transistors (Vtn < Vin < Vdd - |Vtp|). To estimate this current, a simplified model (Figure 6.3) can be employed. Here, τ represents the rise and fall times of the input (assumed to be equal), and the inverter is considered symmetrical.

Short-circuit power dissipation is influenced by several factors. Clock frequency plays a crucial role, as it determines the number of output transitions per second, directly impacting the short-circuit current. Additionally, the rise and fall times of the input signal are proportional to the short-circuit current, as shown in Figure 6.4. Steeper slopes (faster transitions) lead to higher currents.

Power supply scaling offers a significant advantage in mitigating short-circuit power due to the cubic dependence of the current on VDD. Lowering the supply voltage drastically reduces short-circuit current, as shown in Figure 6.5.

However, there are trade-offs to consider. While increasing the load capacitance (Cload) reduces short-circuit current, it also slows down the circuit. A well-balanced approach involves designing for equal input and output slopes.

In conclusion, short-circuit power dissipation necessitates careful design considerations in VLSI circuits. Optimizing input rise/fall times, minimizing clock frequency when possible, and strategic use of load capacitance are all crucial strategies. Furthermore, voltage scaling remains a powerful tool for low-power design due to its significant impact on short-circuit power reduction. By understanding and addressing these factors, researchers can create more energy-efficient VLSI circuits, paving the way for longer battery life and improved performance in portable electronic devices.

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## Static Leakage Power: A Growing Threat in Low-Power VLSI Design

Traditionally, dynamic power dissipation caused by circuit activity has been a primary focus in low-power VLSI design. However, with the miniaturization trend leading to deep-submicron devices, static leakage power is emerging as a significant and growing concern. Unlike dynamic power, which only occurs during circuit operation, static leakage refers to the continuous power dissipation even when the circuit is inactive.

This leakage arises from various mechanisms occurring within transistors, as depicted in Figure 6.17. Some key leakage components include:

1. **Reverse-bias junction leakage:** Leakage currents flow through the reverse-biased junctions formed by transistors, even when they are off. In deep-submicron devices, tunneling effects can further exacerbate this leakage.
2. **Subthreshold leakage:** When the gate voltage (Vgs) is lower than the threshold voltage (Vt), a small current persists between the source and drain of the transistor. This leakage becomes more significant as the threshold voltage is scaled down for performance reasons.

While these individual leakage currents may seem negligible, the cumulative effect across millions of transistors in a VLSI chip can be substantial. This highlights the growing importance of static leakage power in the overall power consumption profile of modern circuits.

Mitigating static leakage power remains a critical aspect of achieving energy-efficient VLSI design, particularly for battery-powered portable devices

// cmos power disss.

// I9 core processor

The **Core i9 processor** represents the pinnacle of modern computing power, boasting impressive performance and cutting-edge features. As compare it to the **Intel 4004 microprocessor**, which was a groundbreaking achievement in its own time.

1. **Operational Voltage**:
   * The **4004 microprocessor** operated at a relatively high voltage range of **5-15V**.
   * In contrast, the **Core i9** operates at an incredibly low voltage of just **1V**. This reduction in voltage not only minimizes power dissipation but also helps prevent device breakdown.
2. **Drawn Length**:
   * The **4004** had a drawn length of approximately **10 micrometers**.
   * Thanks to advancements in semiconductor manufacturing, the **Core i9** has scaled down to an impressive **32/45 nanometers**. This reduction in size contributes to improved performance and efficiency.
3. **Clock Speed**:
   * The **Core i9** boasts clock speeds ranging from **3 to 3.5 GHz**, allowing for lightning-fast processing.
   * In comparison, the clock speed of the **4004** was significantly lower.
4. **Transistors**:
   * The **Core i9** is a marvel of complexity, housing approximately **780 million transistors**.
   * By contrast, the **4004 microprocessor** had a mere **2300 transistors**, despite occupying a similar chip area.
5. **Trade-offs and Challenges**:
   * The reduction in drawn length, while beneficial, poses challenges. It leads to a shorter distance between the source and drain in transistors, potentially compromising control.
   * Using multiple transistors within the same chip area increases parasitic capacitance, contributing to higher power dissipation.
   * Lowering the power supply reduces the electric field but may impact overall chip performance.
   * The increased clock frequency also contributes to higher power dissipation.
6. **Low Power Design**:
   * To address these flaws, low-power design techniques become indispensable. Balancing performance, efficiency, and reliability is crucial.

In summary, while the **Core i9** represents the pinnacle of modern computing, it stands on the shoulders of historical achievements like the **4004 microprocessor**. Advances in technology have allowed us to create powerful processors while overcoming inherent challenges. 🚀💻

Introduction :

Due to the growing demand for portable and battery-powered devices, minimizing power consumption in VLSI design has become a crucial challenge. While CMOS technology offers excellent scaling properties and inherently low static power dissipation, two main components contribute to power usage during signal switching: dynamic current for charging the circuit and short-circuit current that flows briefly when both transistors conduct simultaneously. Understanding these sources and their impact on frequency is essential for designing power-efficient VLSI chips.

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The ever-growing demand for portable and battery-powered electronics has thrust low-power design into the spotlight of VLSI development. While CMOS technology boasts excellent scaling properties and inherently low static power dissipation, challenges remain. During signal switching, two main culprits emerge: dynamic current used to charge the circuit, and short-circuit current that flows briefly when both transistors conduct simultaneously. Understanding these sources and their influence on factors like frequency is paramount in crafting power-efficient VLSI chips. . Understanding these sources and their impact on frequency is essential for designing power-efficient VLSI chips.

// SWitchng power

**Refining Switching Power Dissipation Calculations in VLSI Circuits**

The passage you provided delves into the concept of switching power dissipation in VLSI circuits, a crucial factor in low-power design. It highlights the limitations of the basic formula and proposes a more comprehensive approach.

Here's a breakdown of the key points:

1. **Switching Power Dissipation:** Defined as the power lost during transitions between logic states (0 and 1) in digital circuits. It's the dominant form of power dissipation [2].
2. **Basic Formula (Limitations):**
   * The initial formula (Equation 1 or 2) calculates switching power based on load capacitance (Cload), supply voltage (Vdd), and operating frequency (f).
   * This formula assumes only one transition per clock cycle, which isn't always true in real-world scenarios.
3. **Node Transition Factor (α):**
   * Introduced to account for the actual number of transitions (α) occurring at each clock cycle.
   * The refined formula (Equation 3) incorporates α, providing a more accurate estimate.
4. **Beyond Load Capacitance:**
   * The concept of Cload is limited for complex logic gates where multiple internal nodes experience transitions.
   * Equation 4 addresses this by considering the capacitance (Ci), voltage (Vi), and transition factor (αTi) of each individual node.
   * The summation across all nodes (i=1 to total nodes) provides a more comprehensive picture of switching power dissipation.

This approach offers a more realistic representation of switching power dissipation in VLSI circuits by accounting for factors beyond the basic load capacitance. It emphasizes the importance of considering internal node transitions and their impact on overall power consumption.

// short

1. INTRODUCTION

The ever-growing demand for portable and battery-powered electronics has thrust low-power design into the spotlight of VLSI development. While CMOS technology boasts excellent scaling properties and inherently low static power dissipation, challenges remain. During signal switching, two main culprits emerge: dynamic current used to charge the circuit, and short-circuit current that flows briefly when both transistors conduct simultaneously. Understanding these sources and their influence on factors like frequency is paramount in crafting power-efficient VLSI chips. . Understanding these sources and their impact on frequency is essential for designing power-efficient VLSI chips.

1. POWER DISSIPATION

Power Dissipation in VLSI Circuits: A Balancing Act

Power dissipation remains a critical challenge in achieving high integration levels in VLSI design. While CMOS technology offers excellent scaling properties and low power consumption, understanding the various power dissipation mechanisms is crucial for efficient circuit design.

This research explores the three main contributors to power dissipation in CMOS circuits: dynamic, short-circuit, and static power.

*A. Dynamic Power*

 This component arises from charging and discharging the load capacitance *(CL)* during signal transitions. It is primarily influenced by *CL*, supply voltage *(VDD),* activity factor (*α*, representing the average switching frequency), and clock frequency *(f)*. The formula

*Pdyn = CL ×VDD 2× α × f*

captures this relationship. [5][ 6]

*1) Switching Power Dissipation*

Switching power dissipation is a critical factor limiting battery life and necessitating low-power design approaches in VLSI circuits. It arises from the charging and discharging of the capacitive load at the output of each logic gate during transitions between logic states [2]. The exact value of this load capacitance depends on several parameters, including the fan-out of the gate, its output capacitance, and the wiring capacitances involved [1]. These parameters are all influenced by the underlying fabrication technology generation.

A simplified model can be used to estimate the switching power dissipation. Consider a standard CMOS inverter driving a load capacitance *(CL)* (Figure 6.8a). As the input to the inverter changes, the PMOS or NMOS network conducts accordingly, charging or discharging the capacitor (Figures 6.8b and 6.8c). During charging (from low to high), power is drawn from the supply to accumulate energy in the capacitor. Conversely, power is dissipated during discharging (from high to low).

While a basic formula (Equation 1 or 2) can be derived based on load capacitance, supply voltage *(VDD)*, and operating frequency *(f)*, it assumes only one transition per clock cycle. In reality, logic gates can experience multiple transitions, necessitating a more nuanced approach.

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Furthermore, for complex logic gates, internal nodes besides the output can also undergo transitions during operation. To account for this, a more comprehensive formula (Equation 4) considers the capacitance *(Ci)*, voltage *(Vi)*, and transition factor *(αTi)* of each individual node. The summation across all nodes provides a more holistic picture of switching power dissipation in VLSI circuits.

By understanding and optimizing switching power dissipation through techniques like voltage scaling, designers can achieve significant power reduction in VLSI chips, leading to longer battery life and improved performance in portable electronic devices.

*2)Glitching Power*

The Pitfall of Non-Ideal Delays in VLSI Circuits. Our previous discussions on power consumption assumed gates with zero delay. In reality, gates have finite delays, and these delays can introduce unintended behaviour. These unwanted transitions at the output are known as glitches.

In static CMOS circuits, glitches can occur on the output node or even internal nodes before they reach a stable logic level. Figure 6.15 serves as an example. Ideally, with zero gate delay, the output should remain at 0 when inputs ABC change from 101 to 000. However, with a unit gate delay in the first stage, the output O1 lags behind the C input. This lag causes a temporary switch to the 1 logic level for the duration of the gate delay. This unnecessary transition increases the dynamic power consumption, and this additional power is known as glitching power.

Fortunately, there are techniques to minimize glitching power. One approach involves balancing delays throughout the circuit (Figure 6.16b). This ensures that all signals arrive at their destinations at similar times, minimizing the window for glitches to occur.

For highly loaded nodes (nodes driving a large number of other circuits), buffers can be inserted to balance delays. Additionally, whenever possible, designers may opt for non-cascaded implementations to further reduce glitching power.

*3)Short-Circuit Power Dissipation*

Beyond switching and glitching power, short-circuit power dissipation emerges as another challenge in achieving low-power VLSI design. This phenomenon arises due to the finite rise and fall times of input signals in CMOS logic gates. During these transitions, a brief period exists where both the PMOS and NMOS transistors are partially ON simultaneously. This creates a direct path between the power supply (VDD) and ground (GND), leading to a surge in current flow.

Figure 6.2 depicts a CMOS inverter, where short-circuit current occurs when the input voltage lies between the threshold voltages of the PMOS and NMOS transistors

*(Vtn < Vin < VDD - |Vtp|).*

Pshort circuit ¼ Isc Vdd,

 To estimate this current, a simplified model (Figure 6.3) can be employed. Here, τ represents the rise and fall times of the input (assumed to be equal), and the inverter is considered symmetrical.

Short-circuit power dissipation is influenced by several factors. Clock frequency plays a crucial role, as it determines the number of output transitions per second, directly impacting the short-circuit current. Additionally, the rise and fall times of the input signal are proportional to the short-circuit current.

Power supply scaling offers a significant advantage in mitigating short-circuit power due to the cubic dependence of the current on *VDD*. However, there are trade-offs to consider. While increasing the load capacitance *(Cload)* reduces short-circuit current, it also slows down the circuit. A well-balanced approach involves designing for equal input and output slopes.

*B. Static Power (Leakage Power)*

 Unlike the previous two components, static power is continuously dissipated even when the circuit is inactive. Leakage currents, influenced by *VDD,* threshold voltage *(Vt)*, and transistor size, are the primary culprits. As process technology scales, leakage becomes a more significant concern, potentially consuming over 30% of total power (refer to [2]). Techniques like MTCMOS (refer to [4]) have been proposed to mitigate leakage in sleep modes.

In conclusion, achieving low-power VLSI design requires careful consideration of all three power dissipation components. By optimizing factors like *VDD*, transistor sizing, and circuit techniques for dynamic and short-circuit power reduction, alongside leakage management strategies, researchers can create energy-efficient circuits that pave the way for longer battery life and improved performance in portable devices.

*Static Leakage Power*: A Growing Threat in Low-Power VLSI Design

Traditionally, dynamic power dissipation caused by circuit activity has been a primary focus in low-power VLSI design. However, with the miniaturization trend leading to deep-submicron devices, static leakage power is emerging as a significant and growing concern.

This leakage arises from various mechanisms occurring within transistors, as depicted in Figure 6.17. Some key leakage components include:

1. *Reverse-bias junction leakage* : Leakage currents flow through the reverse-biased junctions formed by transistors, even when they are off. In deep-submicron devices, tunnelling effects can further exacerbate this leakage.

*2. Subthreshold leakage* : When the gate voltage *(Vgs)* is lower than the threshold voltage *(Vt),* a small current persists between the source and drain of the transistor. This leakage becomes more significant as the threshold voltage is scaled down for performance reasons.

While these individual leakage currents may seem negligible, the cumulative effect across millions of transistors in a VLSI chip can be substantial. This highlights the growing importance of static leakage power in the overall power consumption profile of modern circuits.

Mitigating static leakage power remains a critical aspect of achieving energy-efficient VLSI design, particularly for battery-powered portable devices.

                             CONCLUSION

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[Department Of Electronics & Telecommunication](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Government Engineering College, Raipur 492015, (C.G.), India](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[E-Mail: maanjain2608@Gmail.Com ,  priyanshu72748@Gmail.Com](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

**[Abstract](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[– ChatGPT](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)***

**[Review  on Low-Power Designing in VLSI Chips & Comparing Power Dissipation Across Processor Generations](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)**

***[Keyword-](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)***

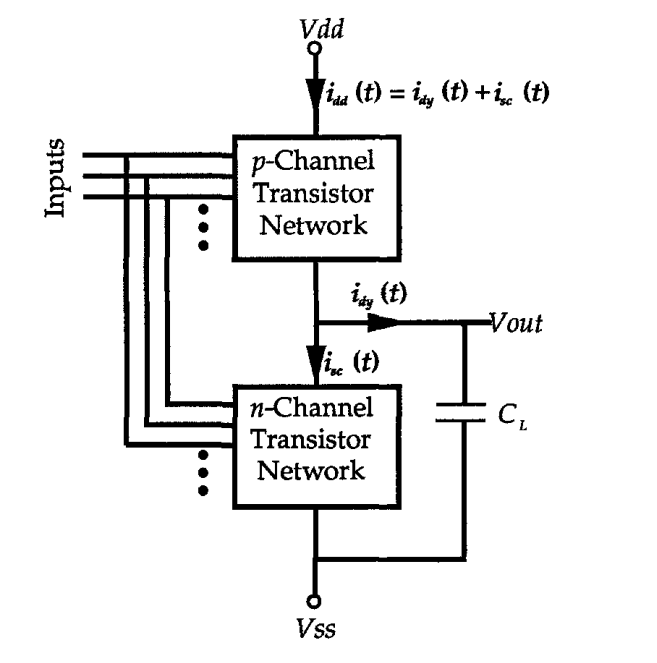
1. [INTRODUCTION](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[The ever-growing demand for portable and battery-powered electronics has thrust low-power design into the spotlight of VLSI development. While CMOS technology boasts excellent scaling properties and inherently low static power dissipation, challenges remain. During signal switching, two main culprits emerge: dynamic current used to charge the circuit, and short-circuit current that flows briefly when both transistors conduct simultaneously. Understanding these sources and their influence on factors like frequency is paramount in crafting power-efficient VLSI chips. . Understanding these sources and their impact on frequency is essential for designing power-efficient VLSI chips.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[[5]](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

1. [POWER DISSIPATION](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Power dissipation remains a critical challenge in achieving high integration levels in VLSI design [2] While CMOS technology offers excellent scaling properties and low power consumption, understanding the various power dissipation mechanisms is crucial for efficient circuit design.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Figure : 1](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[CMOS (Combination of PMOS and NMOS)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[This research explores the two main contributors to power dissipation in CMOS circuits: dynamic  and static power.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

*[A. Dynamic Power](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

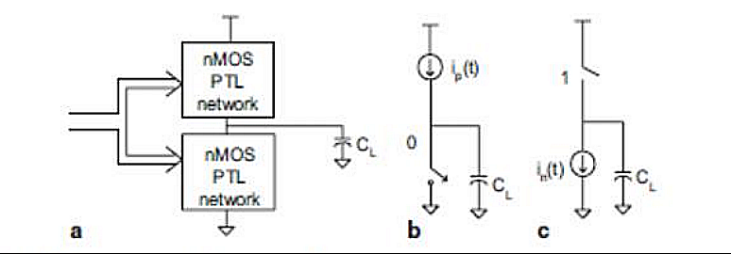
[This component arises from charging and discharging the load capacitance](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(C](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[L](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [during signal transitions. It is primarily influenced by](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[C](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[L](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[, supply voltage](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(V](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[DD](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[),](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [activity factor (](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[α](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[, representing the average switching frequency), and clock frequency](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(f)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[. The formula](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

*[P](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[dyn](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) [= C](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[L](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) [×(V](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[DD](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) [)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[2](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[× α × f](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

[captures this relationship. [2][6][4]](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

*[1) Switching Power Dissipation](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

[Switching power dissipation is a critical factor limiting battery life and necessitating low-power design approaches in VLSI circuits. It arises from the charging and discharging of the capacitive load at the output of each logic gate during transitions between logic states [1]. The exact value of this load capacitance depends on several parameters, including the fan-out of the gate, its output capacitance, and the wiring capacitances involved [7]. These parameters are all influenced by the underlying fabrication technology generation.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

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[figure : 2](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[switching power dissipation model](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[A simplified model (Figure 2a) can be used to estimate the switching power dissipation. Consider a standard CMOS inverter driving a load capacitance](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(C](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[L](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [. As the input to the inverter changes, the PMOS or NMOS network conducts accordingly, charging or discharging the capacitor (Figures 2b and 2c). During charging (from low to high), power is drawn from the supply to accumulate energy in the capacitor. Conversely, power is dissipated during discharging (from high to low).](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[1…….](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[2…….](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[While a basic formula (Equation 1 or 2) can be derived based on load capacitance, supply voltage](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(V](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[DD](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[, and operating frequency](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(f)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[, it assumes only one transition per clock cycle. In reality, logic gates can experience multiple transitions, necessitating a more nuanced approach.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[3………..](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[The concept of the node transition factor](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(α)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [is introduced to account for the actual number of transitions occurring at each clock cycle. This refined formula (Equation 3) provides a more accurate estimate of switching power dissipation.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

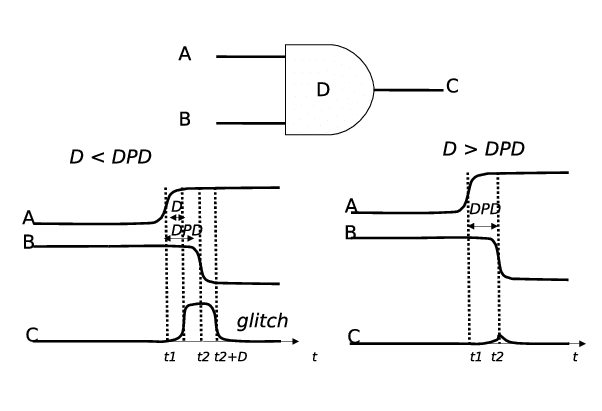
[4………..](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Furthermore, for complex logic gates, internal nodes besides the output can also undergo transitions during operation. To account for this, a more comprehensive formula (Equation 4) considers the capacitance](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(Ci)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[, voltage](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(Vi)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[, and transition factor](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(αTi)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [of each individual node. The summation across all nodes provides a more holistic picture of switching power dissipation in VLSI circuits.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[By understanding and optimizing switching power dissipation through techniques like voltage scaling, designers can achieve significant power reduction in VLSI chips, leading to longer battery life and improved performance in portable electronic devices.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

*[2)Glitching Power](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

[Beyond switching activity and short-circuit power,](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) **[glitching power dissipation](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)** [presents another hurdle in achieving low-power VLSI design. Glitches refer to unwanted, transient voltage fluctuations at the output of a logic gate. These glitches occur due to imbalances in the propagation delays of various input signals within a combinational circuit.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Figure:3                    Glitch power dissipation](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

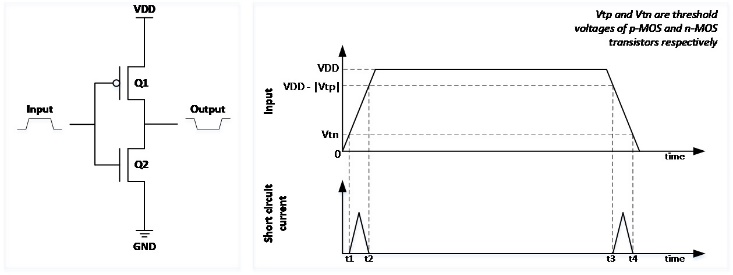
[The figure you sent is indeed a glitch power dissipation curve [1]. It depicts the power dissipated by a glitch in a transistor circuit. The x-axis represents time (t), while the y-axis represents power dissipation (D).](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[The curve shows a voltage glitch, which is a short-duration unintended voltage spike that occurs on a signal line. The glitch causes a surge in power dissipation (DPD) that lasts for a short period (t1 to t2) before settling back to zero. The curve suggests that the higher the glitch amplitude (the difference between A and B), the greater the surge in power dissipation.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Glitch power dissipation is a significant concern in low-power circuit design.  Minimizing glitches can substantially reduce the overall power consumption of a circuit.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

*[3)Short-Circuit Power Dissipation](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

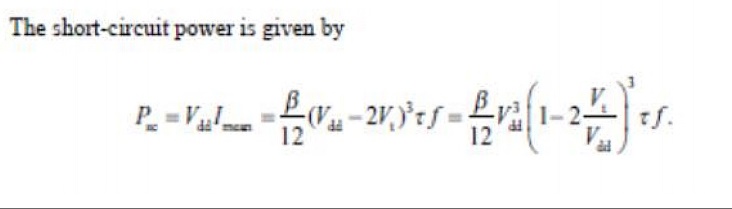
[Beyond switching and glitching power, short-circuit power dissipation emerges as another challenge in achieving low-power VLSI design. This phenomenon arises due to the finite rise and fall times of input signals in CMOS logic gates. During these transitions, a brief period exists where both the PMOS and NMOS transistors are partially ON simultaneously. This creates a direct path between the power supply (V](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[DD](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[) and ground (GND), leading to a surge in current flow.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

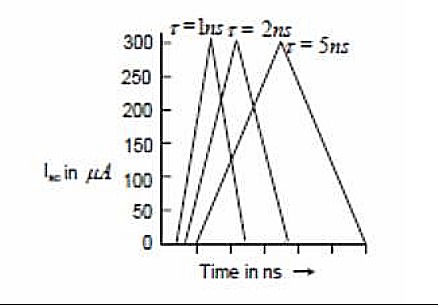
*[](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

*[Figure : 4](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

*[Short-circuit leakage current in an inverter](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

[Figure (4) depicts a CMOS inverter, where short-circuit current occurs when the input voltage lies between the threshold voltages of the PMOS and NMOS transistors](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

*[//formula](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

*[As the clock frequency decides how many times the output changes per second, the short-circuit power is proportional to the frequency. The short- circuit current is also proportional to the rise and fall times. Short-circuit currents for different input slopes are shown in Fig. 5 ](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

*[Figure : 5](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

[To estimate this current, a simplified model (Figure 5 ) can be employed. Here, τ represents the rise and fall times of the input (assumed to be equal), and the inverter is considered symmetrical.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

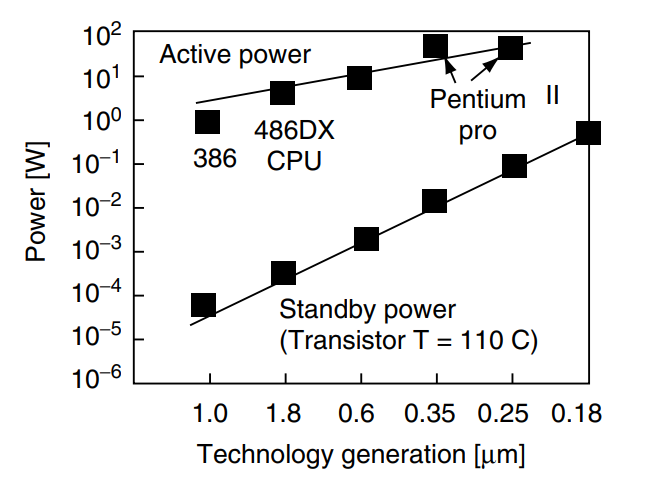
[Short-circuit power dissipation is influenced by several factors. Clock frequency plays a crucial role, as it determines the number of output transitions per second, directly impacting the short-circuit current. Additionally, the rise and fall times of the input signal are proportional to the short-circuit current.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Power supply scaling offers a significant advantage in mitigating short-circuit power due to the cubic dependence of the current on](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[V](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[DD](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[. However, there are trade-offs to consider. While increasing the load capacitance](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(C](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[load](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [reduces short-circuit current, it also slows down the circuit. A well-balanced approach involves designing for equal input and output slopes.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

*[B. Static Power (Leakage Power)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

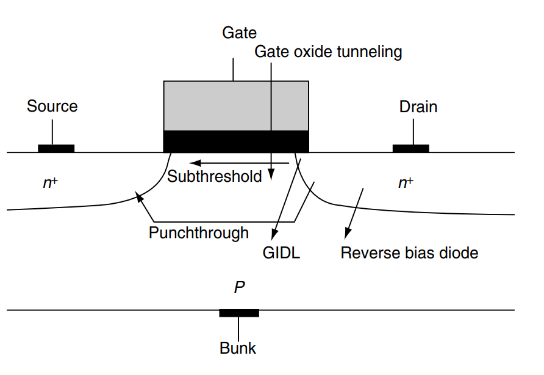
[A Growing Threat in Low-Power VLSI Design .Unlike the previous three components, static power is continuously dissipated even when the circuit is inactive. Leakage currents, influenced by](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[V](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[DD](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[,](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [threshold voltage](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(V](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[t](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*[, and transistor size, are the primary culprits. As process technology scales, leakage becomes a more significant concern, potentially consuming over 30% of total power (refer to [2]).](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Traditionally, dynamic power dissipation caused by circuit activity has been a primary focus in low-power VLSI design. However, with the miniaturization trend leading to deep-submicron devices, static leakage power is emerging as a significant and growing concern.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[There is reduction in static power dissipation with each passing year , as depicted in Figure 6](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Figure : 6](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Static Power Evolution with Respect to Technology](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Figure : 7  The Different Sources of Leakage Current in MOS Transistors ](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Some key leakage components include:](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

*[1.Reverse-bias junction leakage](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [: Leakage currents flow through the reverse-biased junctions formed by transistors, even when they are off. [10] In deep-submicron devices, tunnelling effects can further exacerbate this leakage.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

*[2.Subthreshold leakage](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [: When the gate voltage](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(V](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[gs](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [is lower than the threshold voltage](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) *[(V](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[t](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[),](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)* [a small current persists between the source and drain of the transistor. This leakage becomes more significant as the threshold voltage is scaled down for performance reasons [9].](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[While these individual leakage currents may seem negligible, the cumulative effect across millions of transistors in a VLSI chip can be substantial. This highlights the growing importance of static leakage power in the overall power consumption profile of modern circuits.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[Mitigating static leakage power remains a critical aspect of achieving energy-efficient VLSI design, particularly for battery-powered portable devices.](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

1. *[Comparing (4th and 14th gen) Processors](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)*

[Core i7 processor is a state of the art processor and is the latest and fastest processor present today. The i7 4th Generation the processor had an operational voltage of 1.72V while having 2.6 Billion transistors ,and base frequency of 3.4 GHz had a leakage of 150μA .But after a decade of development, the i7 14](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)[th](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) [gen. having over 48 billion transistors ,  an operational voltage of 1V, which reduces the power dissipation. Also, it reduces the electric field and will prevent the device from breaking down. The drawn length is also reduced from 10micro in the 4004 microprocessor to 32/45 nanometer in Intel i7, all thanks to scaling. Also, the clock speed has been increased to 3-3.5 GHz. The i7 has approximately 780 million transistors, while the 4004 microprocessor has only 2300, while keeping the chip area the same. But these techniques have their own cons. Reduction of drawn length leads to a reduced distance between the source and the drain, leading to loss of control of the transistor. Also, using multiple transistors while keeping the chip area the same leads to a significant increase in the parasitic capacitance (which in turn leads to an increase in power dissipation). While reducing power supply we can reduce electric field, but it will affect the overall performance of the chip, i.e. reduce it. The increase in clock frequency will also lead to an increase in the transition factor, and both will together contribute to an increase in the power dissipation. Hence, low power designing and its techniques are indispensable to overcome these flaws[11].](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[CONCLUSION](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[REFERENCES](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[[1]Low Power designing in VLSI chips Navneesh Singh Malhotra ,2015 International Conference on Advances in Computer Engineering and Applications (ICACEA) IMS Engineering College, Ghaziabad, India (ISBN:978-1-4673-6911-4)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[[2] Low-Power, High-Speed CMOS VLSI Design by Tadahiro Kuroda; IEEE 2002 international conference proceedings.  (ISSN: 1063-6404)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[[3] Power Dissipation of VLSI Array Processing Systems\* Paul M.Chau and Scott R. Powell, 1992  Journal of VLSI Signal Processing, 4, 199-212 (1992) 9 1992](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

[[4]](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG) [[Trends in low-power VLSI desig](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)](https://www.academia.edu/download/45225929/The_Electrical_Engineering_Handbook.pdf#page=282)[n ,T Darwish, M Bayoumi - The Electrical Engineering Handbook, 2005(ISBN: 0-12-170960-4)](https://1.bp.blogspot.com/-jCsf39G06LQ/XhI3LxTlUDI/AAAAAAAAiMY/jaC-l6YOU0ko2a_DPyayQ7unwRP-7heswCLcBGAsYHQ/s1600/27.PNG)

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